Total No. of Printed Pages—6

3 SEM TDC PHYH (CBCS) C 7

2021

(Held in January/February, 2022)

PHYSICS

(Core)

Paper : C–7

(Digital Systems and Applications)

Full Marks : 53

Pass Marks : 21

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct option : 1×5=5

(a) In a CRT, the focus can be controlled by

(i) adjusting the positive potential of the anode

(ii) adjusting the negative potential of the grid

(iii) adjusting the d.c. potential of the horizontal deflection plates

(iv) adjusting the d.c. potential of the vertical deflection plates

(b) The binary equivalent of the decimal number 52·875 is

(i) 100110.101

(ii) 100100.110

(iii) 110100.111

(iv) 111010.011

(c) The maxterm which is missing in the expression $A(\overline{B} + A)B$ is

(i) M_0

(ii) M_1

(iii) M_2

(iv) M_3

(d) Which of the following is ***not*** correct?

(i) $\overline{A \oplus B} = \overline{A} \oplus B$

(ii) $A \oplus B = \overline{A} \oplus \overline{B}$

(iii) $A + BC = (A + B)(A + C)$

(iv) $A \oplus \overline{A} = 0$

(e) When a flip-flop is reset, its outputs will be

(i) $Q = 0, \overline{Q} = 0$

(ii) $Q = 1, \overline{Q} = 0$

(iii) $Q = 0, \overline{Q} = 1$

(iv) $Q = 1, \overline{Q} = 1$

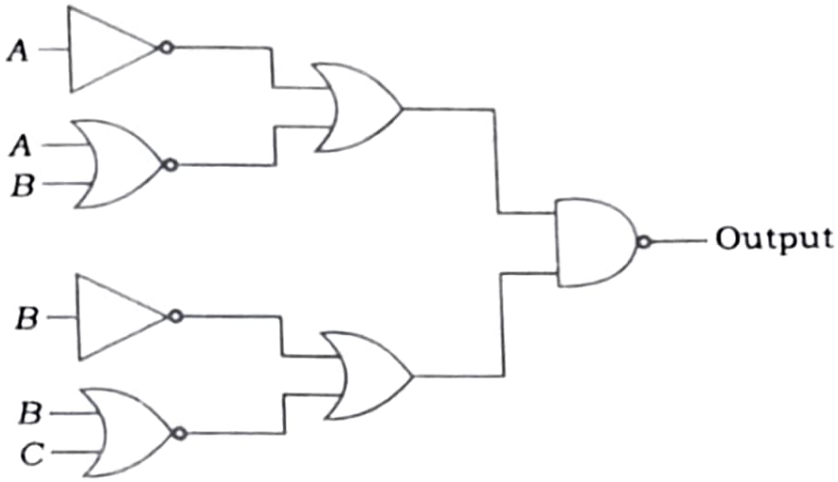
2. Draw the block diagram of a general purpose CRO and mention the different parts. 2

3. What are different scales of integration? Mention the number of components in each scale of integration. 2

4. (a) Describe how NAND gate can be used to realize XOR gate. 3

(b) Draw the logic diagram and write the truth table of an even parity bit generator using XOR gate (consider 4-bit input). 2

5. Draw the simplest possible logic diagram that implements the output of the logic diagram shown below : 3



Or

Reduce the expression $f = \Sigma m(0, 2, 3, 4, 5, 6)$ using K-map and implement it using AOI logic. 2+1=3

6. Draw the logic diagram of a decimal to BCD encoder and explain its working. 2+2=4

7. *(a)* Describe the 2's complement method of subtraction. 2

(b) What is half adder? Draw the logic diagram for half adder using only NAND gates. 1+2=3

8. How does a *J-K* flip-flop differ from an *S-R* flip-flop in its operation? Draw the logic diagram of an active-high *S-R* latch using only NAND gates and describe its operation. 1+3=4

Or

What is race around condition in flip-flop? Explain how master-slave flip-flops can eliminate this condition. 1+3=4

9. Draw the functional block diagram of an IC-555 and explain the function of each pin. 3

10. Draw the logic diagram of 4-bit serial-in, parallel-out shift register using *D* flip-flops. 2

11. What is ring counter? Describe the working of a 4-bit ring counter. 1+3=4

Or

What is synchronous counter? Describe the procedure for systematic design of any synchronous counter. 1+3=4

12. (a) What are different types of secondary memory? Write one advantage of DDR RAM. 1+1=2

(b) Explain the functions of different buses present in a computer. 3

13. (a) What are the various registers of 8085 microprocessor? 2

(b) Describe the different types of addressing modes of 8085 microprocessor. 4

Or

Draw the simplified block diagram of 8085 microprocessor showing the main units. 4

14. Define opcode and operant. Explain the arithmetic instruction of 8085 with example. 1+2=3

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